AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

1. (currently amended) A semiconductor device comprising:

an insulator layer;

a conductive plug positioned within said insulator layer and formed of a single conductive material;

a doped region connected to said conductive plug;

an etch-stop layer located on said insulator layer and surrounding said plug;

a non-conductive layer having ~~an etched~~ at least a first and a second etched via formed at least partially over said conductive plug, wherein said first etched via is wider in diameter than said conductive plug; and

a conductive connector formed in said via in electrical contact with said plug and including a first conductive layer deposited in and in contact with said etched via and a second conductive layer deposited over and in contact with said first conductive layer, said first conductive layer including a portion in contact with said conductive plug.

2. (canceled)

3. (original) The semiconductor structure of claim 1, wherein said etch-stop layer comprises silicon nitride.

4. (original) The semiconductor structure of claim 1, wherein said etch-stop layer comprises silicon carbide.

5. (original) The semiconductor structure of claim 1, wherein said etch-stop layer comprises silicon dioxide.

6. (original) The semiconductor structure of claim 1, wherein said etch-stop layer comprises silicon nitride and silicon carbide.

7. (original) The semiconductor structure of claim 1, wherein said non-conductive layer comprises doped silicate glass.

8. (original) The semiconductor structure of claim 7, wherein said doped silicate glass comprises borophosphosilicate glass.

9. (previously presented) The semiconductor structure of claim 1, wherein said first conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

10. (original) The semiconductor structure of claim 1, further comprising a substrate with a connection region, wherein said conductive plug is provided over said connection region.

11. (previously presented) A semiconductor device comprising:

at least one memory cell comprising:

an active region in a substrate;

a conductive plug formed of a single conductive material positioned within an insulator layer and provided over said active region, said conductive plug being electrically connected with said active region;

an etch-stop layer deposited on said insulator layer and around said conductive plug;

an intermediate non-conductive layer provided over said etch stop layer having at least a first and a second etched via over said plug, said first etched via being

wider in diameter than said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

a first conductive layer deposited in and in contact with said first and second vias, said first conductive layer including a portion in contact with said conductive plug, and a second conductive layer deposited over and in contact with said first conductive layer.

12. (canceled)

13. (previously presented) The semiconductor memory device of claim 11, wherein said intermediate layer comprises doped silicate glass.

14. (previously presented) The semiconductor memory device of claim 13, wherein said doped silicate glass comprises borophosphosilicate glass.

15. (previously presented) The semiconductor memory device of claim 11, wherein said first conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

16. (previously presented) The semiconductor memory device of claim 11, wherein said second conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

17. (previously presented) The semiconductor memory device of claim 11, further comprising a plurality of said memory cells.

Claims 18-24 (canceled).

25. (previously presented) A processor-based system comprising:

a processing unit;

a semiconductor circuit coupled to said processing unit, said semiconductor circuit comprising:

a conductive plug formed of a single conductive material positioned within an insulator and provided on a connection region;

an etch-stop layer deposited on said insulator, said etch-stop layer being at the same level as a top portion of said conductive plug;

an intermediate non-conductive layer provided over said etch-stop layer having at least a first and a second etched via over said conductive plug, said first etched via being wider in diameter than said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

a conductive connector electrically coupled to said connection region, said conductive connector comprising a first conductive layer deposited in and in contact with said first and second etched vias, said first conductive layer including a portion in contact with said conductive plug, and a second conductive layer deposited over and in contact with said first conductive layer.

26. (canceled)

27. (previously presented) The processor-based system of claim 25, wherein said connection region comprises a doped region within said substrate.

28. (previously presented) The processor-based system of claim 25, wherein said intermediate layer comprises doped silicate glass.

29. (original) The processor-based system of claim 28, wherein said doped silicate glass comprises borophosphosilicate glass.

30. (previously presented) The processor-based system of claim 25, wherein said first conductive layer comprises at least one layer of one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

31. (previously presented) The processor-based system of claim 25, wherein said second conductive layer comprises at least one layer of one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

32. (previously presented) The processor-based system of claim 25, further comprising a substrate, and wherein said connection region is located in said substrate, and wherein said conductive plug is located over said connection region.

Claims 33-38 (canceled).

39. (previously presented) The semiconductor memory device of claim 17, wherein said plurality of said memory cells are in an array.